

INTRODUCTION

- OVERVIEW OF

ROCKWELL R6500

MOTOROLA 6800

INTEL 8080 FAMILIES

- FACTORS INFLUENCING MICROPROCESSOR
SELECTION

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OVERVIEW OF CHIP FAMILIES

- MICROPROCESSORS
- MEMORIES
- I/O CIRCUITS
- SUPPORT CIRCUITS

OVERVIEW OF MICROPROCESSORS

• FEATURES

	ROCKWELL 6500	MOTOROLA 6800	INTEL 8080A
— WORD LENGTH	8 BIT PARALLEL	8 BIT PARALLEL	8 BIT PARALLEL
— CLOCK RATE	1, 2 MHZ TO 40 KHZ	1.0 MHZ TO 100 MHZ	2 MHZ TO 500 KHZ
— MEMORY ADDRESSES	64K	64K	64K
— I/O ADDRESSES	0	0	256 INPUT + 256 OUTPUT
— BASIC INSTRUCTIONS	56	72	69
— REAL ADDRESSING MODES	13	8	6
— ARITHMETIC ACCUMULATORS (8 BIT)	1	2	1
— SCRATCH REGISTERS (8 BIT)	0	0	6
— INDEX REGISTERS (16 BIT)	2 (8 BIT REG)	1	0
— TOTAL WORKING REGISTERS (8 BIT)	4	4	7
— HARDWARE INTERRUPTS	2	2	1 (EASILY VECTORED TO 8 LOCATIONS)
— POWER SUPPLIED	+5 VOLTS DC	+5 VOLTS DC	+5, -5, +12 VOLTS DC

INTERNAL ORGANIZATION

- BLOCK DIAGRAM — DATA FLOW
- REGISTERS
- FLAGS
- STACK FEATURES
- INTERRUPT HANDLING
- DIRECT MEMORY ACCESS
- COLD START AND OTHER ARCHITECTURAL CONSIDERATIONS

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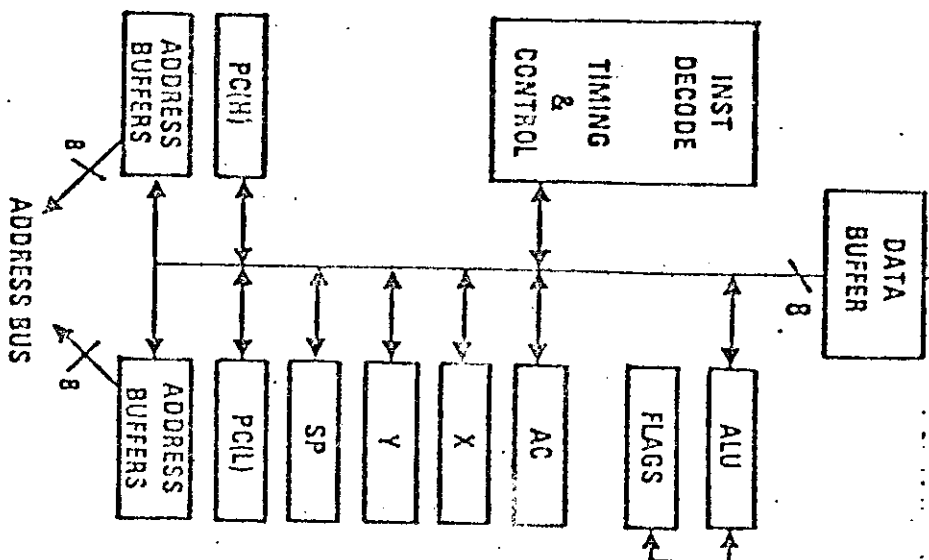
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BLOCK DIAGRAMS

ROCKWELL

6500

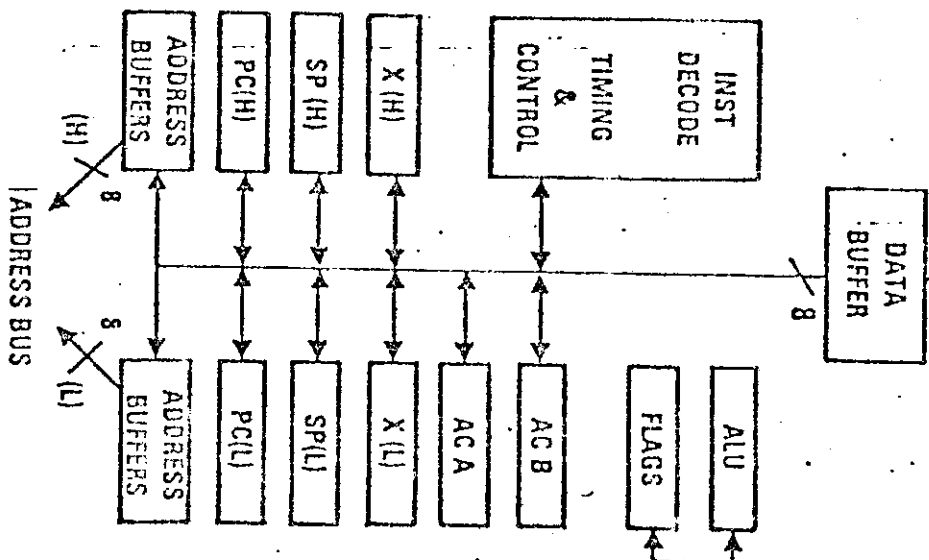
EXTERNAL DATA BUS



MOTOROLA

6800

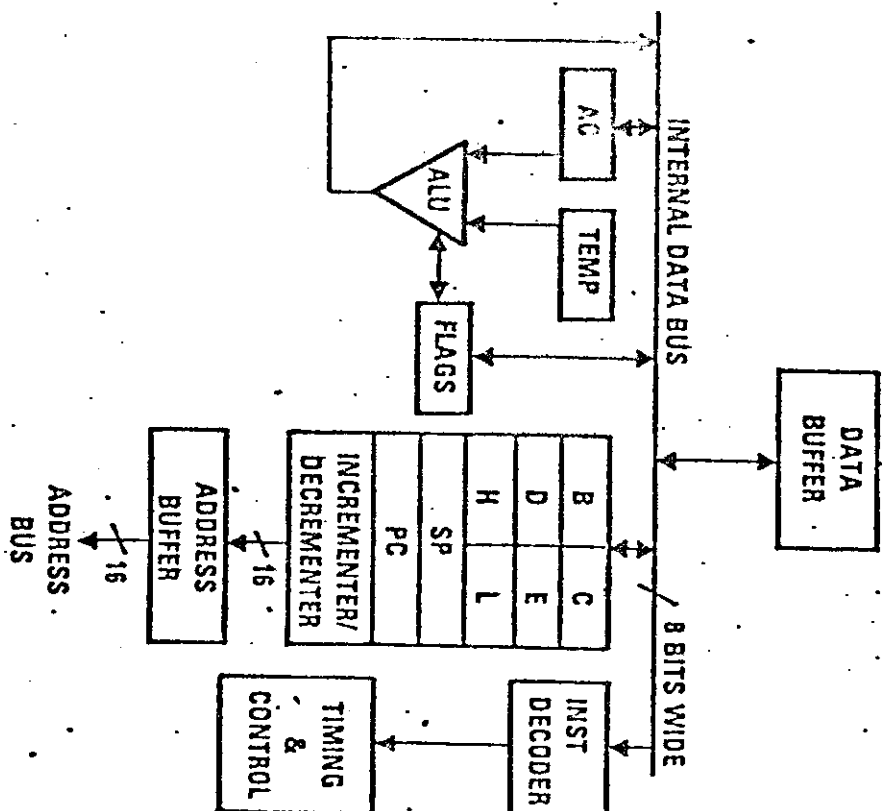
EXTERNAL DATA BUS



INTEL

8080

EXTERNAL DATA BUS



REGISTERS

ROCKWELL

6500

MOTOROLA

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INTEL

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- 1 8-BIT ACCUMULATOR

- 2 8-BIT ACCUMULATORS

- EASES DOUBLE PRECISION (16-BIT) ARITHMETIC

- 1 8-BIT ACCUMULATOR

- NO SCRATCH PAD

- NO SCRATCH REGISTERS

- 6 8-BIT SCRATCH REGISTERS

- SAVES STORING

- INTERMEDIATE RESULTS

- IN MEMORY

- LIMITED ADDRESSING CAPABILITY

- ENABLES ACCESS TO MULTIPLE LISTS

- 2 8-BIT INDEX REGISTER

- 1 16-BIT INDEX REGISTER
- PSEUDO INDEX REGISTER

- ALLOWS EASY ACCESS TO LISTS, LOOPING

- NO INDEX REGISTER

- 1 8-BIT STACK POINTER

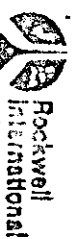
- 1 16-BIT STACK POINTER

- 1 16-BIT STACK POINTER

- 1 16-BIT PROGRAM COUNTER

- 1 16-BIT PROGRAM COUNTER

- 1 16-BIT PROGRAM COUNTER



MICROPROCESSOR REGISTER STRUCTURE

ROCKWELL
6500

MOTOROLA
6800

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FLAGS (7 BITS)	CCR FLAGS (5 BITS)	PSW FR FLAGS (5 BITS)	A ACCUMULATOR(8)
A ACCUMULATOR A(8)	A ACCUMULATOR A(8)	BC B B REG (8)	C C REG (8)
X INDEX X(8)	B ACCUMULATOR B(8)	DE D D REG (8)	E E REG (8)
Y INDEX Y(8)	X INDEX REGISTER (16)	HL H H REG (8)	L L REG (8)
SP STACK POINTER (6)	SP STACK POINTER (16)	SP STACK POINTER (16)	
PC PROGRAM COUNTER (16)	PC PROGRAM COUNTER (16)	PC PROGRAM COUNTER (16)	

FLAGS

ROCKWELL

6500

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- CARRY
- INTERRUPT ENABLE
- SIGN
- DECIMAL MOVE
- ZERO
- OVERFLOW
 - PARITY CHECKING AND GENERATION MUST BE DONE BY SOFTWARE OR EXTERNAL HARDWARE
- HALF CARRY
- INTERRUPT ENABLE
- SIGN
- CARRY
- ZERO
- OVERFLOW (2's COMPLEMENT)
 - PARITY CHECKING AND GENERATION MUST BE DONE BY SOFTWARE OR EXTERNAL HARDWARE
- HALF CARRY
- INTERRUPT ENABLE
 - (NOT IN FLAG REGISTER)
- SIGN
- CARRY
- ZERO
- PARITY
 - PARITY FLAG ENABLES CHECKING AND GENERATING PARITY WITHIN CPU
- OVERFLOW FLAG FACILITATES 2's COMPLEMENT ARITHMETIC
- CHECKING FOR 2's COMPLEMENT OVERFLOW REQUIRES SOFTWARE
- ACCESS TO FLAGS THROUGH ACCUMULATOR A
- ACCESS TO FLAGS THROUGH STACK
- BREAK COMMAND

1

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STACK FEATURES

ROCKWELL

MOTOROLA

INTEL

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PORTION OF RAM IS RESERVED FOR STACK _____

STACK IS ADDRESSED BY AN 8 BIT STACK POINTER _____

STACK POINTER MUST BE INITIALIZED BY PROGRAM _____

PC AND STATUS REGISTERS ARE AUTOMATICALLY SAVED AND REPLACED DURING INTERRUPTS _____

ALL CPU REGISTERS ARE AUTOMATICALLY SAVED AND REPLACED DURING INTERRUPTS _____

RETURN ADDRESS (PC) CAN BE SAVED AND REPLACED DURING INTERRUPTS _____

RETURN ADDRESS IS AUTOMATICALLY SAVED AND REPLACED DURING SUBROUTINE CALLS _____

ACCUMULATOR(S) CAN BE PUSHED IN AND POPPED OFF THE STACK _____

REGISTER PAIRS CAN BE PUSHED IN AND POPPED OFF OF THE STACK _____

STACK CONTENTS CAN BE OPERATED BY PROGRAM _____

STACK INFORMATION IS AVAILABLE FOR DEBUG _____

"UNLIMITED" SUBROUTINE NESTING IS POSSIBLE _____

"UNLIMITED" INTERRUPTS ARE POSSIBLE _____

REENTRANT SUBROUTINES ARE POSSIBLE _____

MULTIPLE STACKS CAN BE CREATED _____

INTERUPT PROCEDURES

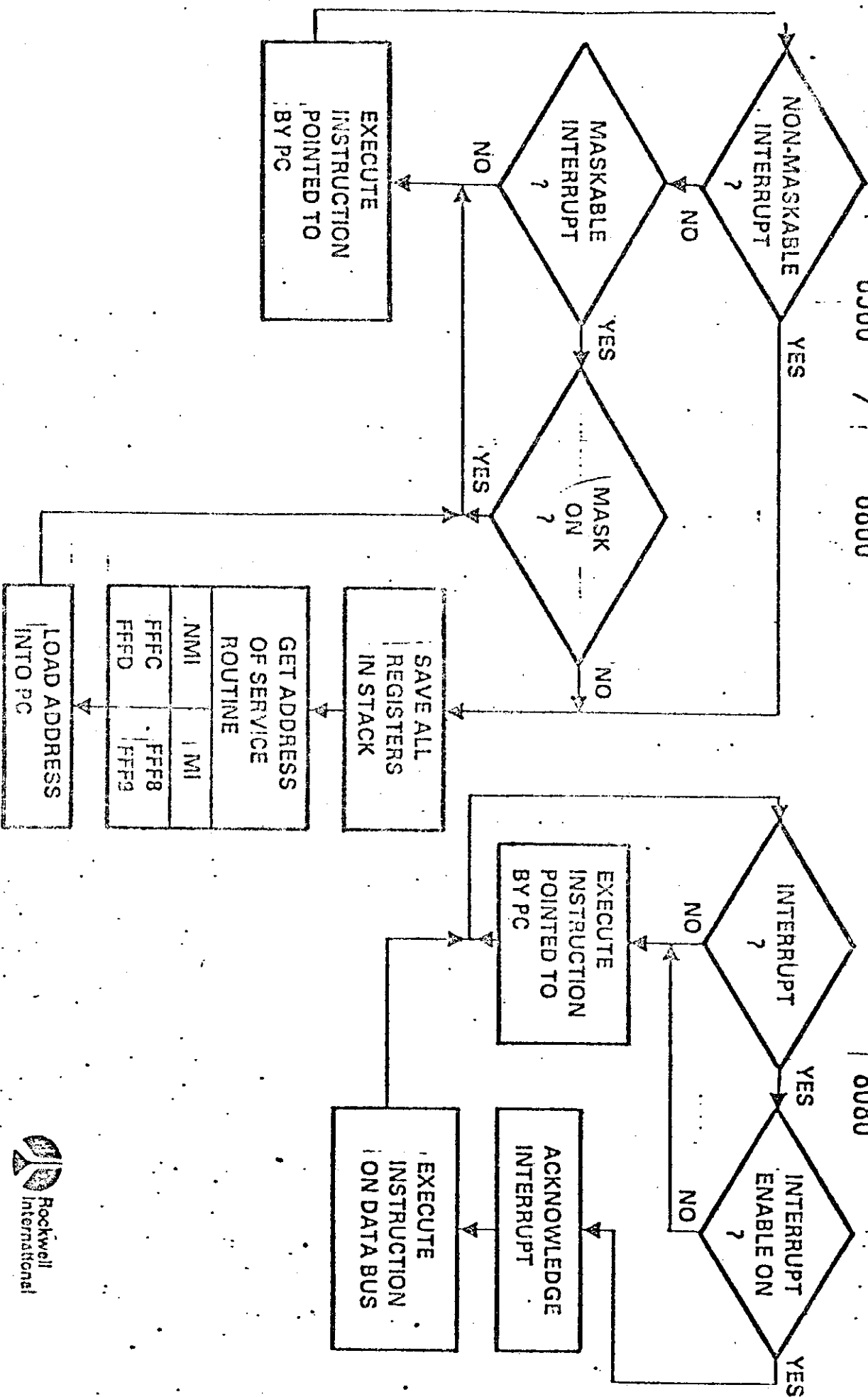
ROCKWELL / MOTOROLA

650-

580

INTEL

8080





INTERRUPT HANDLING

ROCKWELL

6500

MOTOROLA

6800

INTEL

8080

■ _____
— 1 INTERRUPT REQUEST LINE — ■
— MASKABLE

■ 1 INTERRUPT REQUEST LINE
— MASKABLE

■ _____
— 1 INTERRUPT REQUEST LINE — ■
— NON MASKABLE

■ _____
— 1 SOFTWARE INTERRUPT REQUEST — ■
— NON MASKABLE

■ RESTART INSTRUCTION IS SIMILAR
TO SOFTWARE INTERRUPT

■ _____
— 2 VECTORS INHERENT
— 3 VECTORS INHERENT
— UNLIMITED VECTORS POSSIBLE

■ INTERRUPT VECTOR (POINTER TO SERVICE
ROUTINE) MUST BE GENERATED BY
EXTERNAL HARDWARE
— 8 VECTORS EASY
— UNLIMITED VECTORS POSSIBLE

ONLY PC AND STATUS REGISTER
IS SAVED IN STACK
■ _____
■ ALL CPU REGISTERS AUTOMATICALLY SAVED IN STACK
CAN WAIT FOR CRITICAL INTERRUPT WITH CPU
REGISTERS SAVED (WAIT INSTRUCTION)

■ ONLY PC SAVED IN STACK IF RESTART OR
CALL INSTRUCTION IS SUPPLIED BY
EXTERNAL HARDWARE
■ CAN SAVE CPU REGISTERS UNDER PROGRAM
CONTROL, THEN WAIT

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DIRECT MEMORY ACCESS

ROCKWELL

6500

• 3 DMA TECHNIQUES

- READY
- CYCLE STEAL
- SLOW CLOCK AND MULTIPLEX

• SLOWEST DMA RESPONSE

2 μ S @ 1 MHz

MOTOROLA

6800

• 3 DMA TECHNIQUES

- HALF PROCESSOR
- CYCLE STEAL (5 μ S MAX)
- SLOW CLOCK AND MULTIPLEX

• DMA REQUEST MUST BE EXTERNALLY SYNCHRONIZED

• SLOWEST DMA RESPONSE:

13 μ S @ 1 MHz (HALT MODE)

INTEL

8080

• 1 DMA TECHNIQUE

- HALT PROCESSOR

• DMA REQUESTED NEED NOT BE SYNCHRONIZED

• SLOWEST DMA RESPONSE:

2.5 μ S @ 2 MHz

COLD START AND OTHER ARCHITECTURAL CONSIDERATIONS

ROCKWELL

6500

- ON ACTIVATION OF RESET LINE
PROGRAM WILL FETCH NEXT
INSTRUCTION FROM MEMORY
ADDRESS HELD IN LOCATION
FFFC16, FFFD16

MOTOROLA

6800

- ON ACTIVATION OF RESET LINE;
PROGRAM WILL FETCH NEXT
(FIRST) INSTRUCTION FROM
MEMORY ADDRESS HELD IN
LOCATION FFFE₁₆, FFFF₁₆
(SPECIAL ADDRESS DECODING
MAY BE REQUIRED)

INTEL

8080

- ON ACTIVATION OF THE RESET
LINE; PROGRAM WILL FETCH
NEXT (FIRST) INSTRUCTION
FROM LOCATION 0000₁₆

■ SINGLE STEPPING THROUGH _____
PROGRAMS IS POSSIBLE WITH
EXTERNAL HARDWARE

C

C

C

ADDRESSING MODES

• DEFINITIONS

- DIRECT
- EXTENDED
- IMMEDIATE
- INDEXED
- RELATIVE
- REGISTER INDIRECT
- IMPLIED
- REGISTER

• PROCESSOR CAPABILITIES

DEFINITIONS

- DIRECT ADDRESSING

8 8

— AKA: PAGE ZERO ADDRESSING

OP CODE	ADDRESS
---------	---------

— 2 BYTE INSTRUCTION

— SECOND BYTE POINTS TO ABSOLUTE ADDRESS IN FIRST 256 LOCATIONS OF MEMORY

- EXTENDED ADDRESSING

8 8 8

— 3 BYTE INSTRUCTION

— SECOND AND THIRD BYTE POINT TO LOCATION ANYWHERE IN MEMORY

OP CODE	ADDRESS
---------	---------

— (INTEL CALLS THIS DIRECT ADDRESSING)

- IMMEDIATE

8 8

— 2 BYTE INSTRUCTION

— SECOND BYTE IS OPERAND

OP CODE	OPERAND
---------	---------

- IMMEDIATE EXTENDED

8 8 8

— 3 BYTE INSTRUCTION

— SECOND AND THIRD BYTES ARE OPERAND

OP CODE	OPERAND
---------	---------

DEFINITIONS

- REGISTER INDIRECT ADDRESSING

- 1 BYTE INSTRUCTION

- INSTRUCTION SPECIFIED A 16 BIT CPU REGISTER WHICH CONTAINS A POINTER TO ANY LOCATION IN MEMORY

8

OP CODE

- LIKE INDEXED ADDRESSING WITHOUT AN OFFSET

- IMPLIED ADDRESSING

- VARIABLE LENGTH INSTRUCTIONS

- INSTRUCTION IMPLIES ONE OR MORE CPU REGISTERS AS CONTAINING OPERANDS

- (MOTOROLA CALLS THIS INHERENT ADDRESSING

8

OP CODE

- REGISTER ADDRESSING

- VARIABLE LENGTH INSTRUCTIONS

- INSTRUCTION CONTAINS FIELD WHICH SPECIFIES ONE OR MORE CPU REGISTERS AS CONTAINING OPERANDS

8

OP CODE	REG	REG
---------	-----	-----

- ACCUMULATOR ADDRESSING

- DENOTES A ONE BYTE INSTRUCTION OPERATING UPON THE ACCUMULATOR

DEFINITIONS

• INDEXED ADDRESSING

— 2 BYTE INSTRUCTION

8

8

OP CODE	OFFSET
---------	--------

— CONTENTS OF INDEX REGISTER ARE ADDED TO UNSIGNED BINARY NUMBER IN SECOND BYTE TO FORM POINTER TO A LOCATION IN MEMORY WITHIN AN OFFSET OF +0 TO +255 OF THE CONTENTS OF THE INDEX REGISTER

— CONTENTS OF INDEX REGISTER ARE NOT ALTERED

• RELATIVE ADDRESSING

— 2 BYTE INSTRUCTION

8

8

OP CODE	DISP
---------	------

— CONTENTS OF PROGRAM COUNTER ARE ADDED TO 2'S COMPLEMENT NUMBER IN SECOND BYTE FORMING A POINTER TO A LOCATION WITHIN A DISPLACEMENT OF -125 TO + 129 OF THE PRESENT INSTRUCTION

— THE PROGRAM COUNTER IS NOT ALTERED

PROCESSOR ADDRESSING CAPABILITIES

ROCKWELL	MOTOROLA	INTEL
6500	6800	8080

PROCESSORS SAME

- | | | |
|--------------------------|--|----------------------|
| • ABSOLUTE INDIRECT | • EXTENDED | • EXTENDED |
| • ACCUMULATOR ADDRESSING | • REGISTER INDIRECT
INDEXED WITH 0 OFFSET | • REGISTER INDIRECT |
| • IMMEDIATE | • IMMEDIATE | • IMMEDIATE |
| • ABSOLUTE ADDRESSING | • IMMEDIATE EXTENDED | • IMMEDIATE EXTENDED |
| • IMPLIED | • IMPLIED | • IMPLIED |

PROCESSORS DIFFER

- | | | |
|--|--|------------|
| • ZERO PAGE ADDRESSING | • DIRECT | • REGISTER |
| • INDEXED | • INDEXED | |
| INDEXED ZERO PAGE | | |
| INDEXED ABSOLUTE | • RELATIVE | |
| INDEXED INDIRECT | AVAILABLE ONLY WITH
BRANCH INSTRUCTIONS | |
| INDIRECT INDEXED | | |
| • RELATIVE | | |
| AVAILABLE ONLY WITH
BRANCH INSTRUCTIONS | | |

OVERVIEW OF MEMORIES

ROCKWELL

6500

MOTOROLA

6800

INTEL

8080

• READ/WRITE (RAM)

2114 STATIC 1024 X 4

6810A STATIC 128 X 8

8101-2 STATIC 256 X 4

(SEPARATE I/O)

6604 DYNAMIC 4096 X 1 (16 PIN)

8111-2 STATIC 256 X 4

(COMMON I/O)

6605 DYNAMIC 4096 X 1 (22 PIN)

8102 STATIC 1024 X 1

8107 DYNAMIC 4096 X 1

5101 STATIC CMOS 256 X 4

• READ ONLY (ROM)

2316B 2048 X 8

6630 1024 X 8

8302 256 X 8

2332 4096 X 8

6830A 1024 X 8

8308 1024 X 8

68317 2048 X 8

8316 2048 X 8

68308 1024 X 8

8702 256 X 8

• PROGRAMMABLE

HEAD ONLY

NOTE:

68708 1024 X 8

MOTOROLA 6800

8704 512 X 8

(PROM) — ERASABLE

RAMS AND ROMS

8704 1024 X 8

ARE COMPATIBLE

WITH R6500 BUS

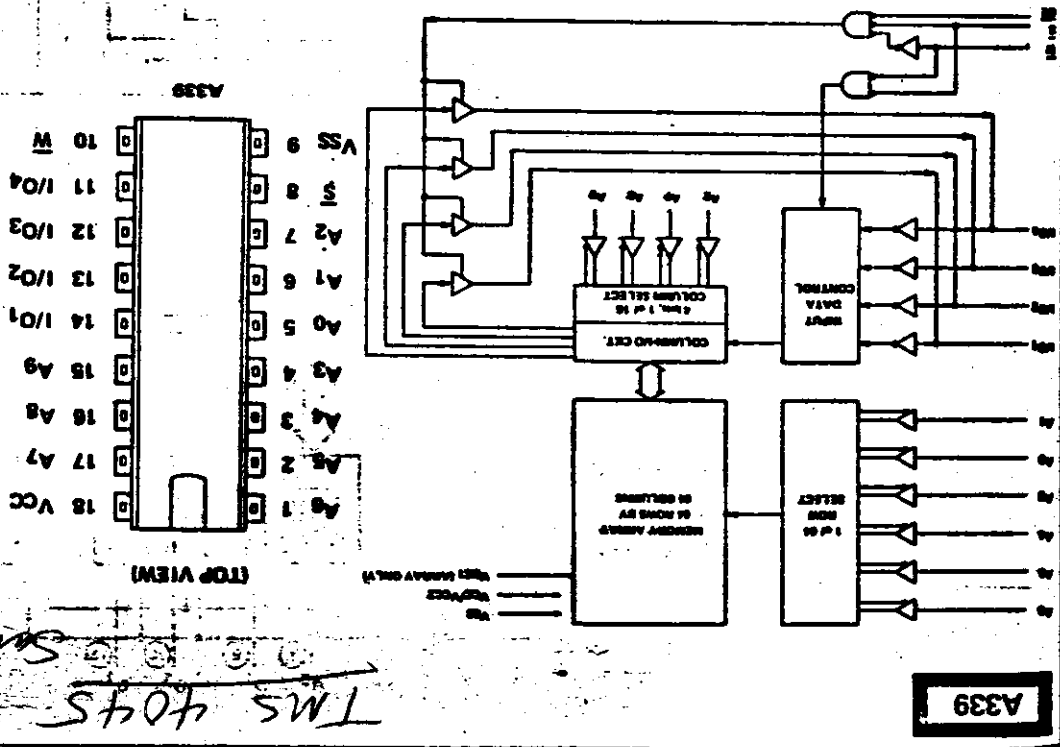


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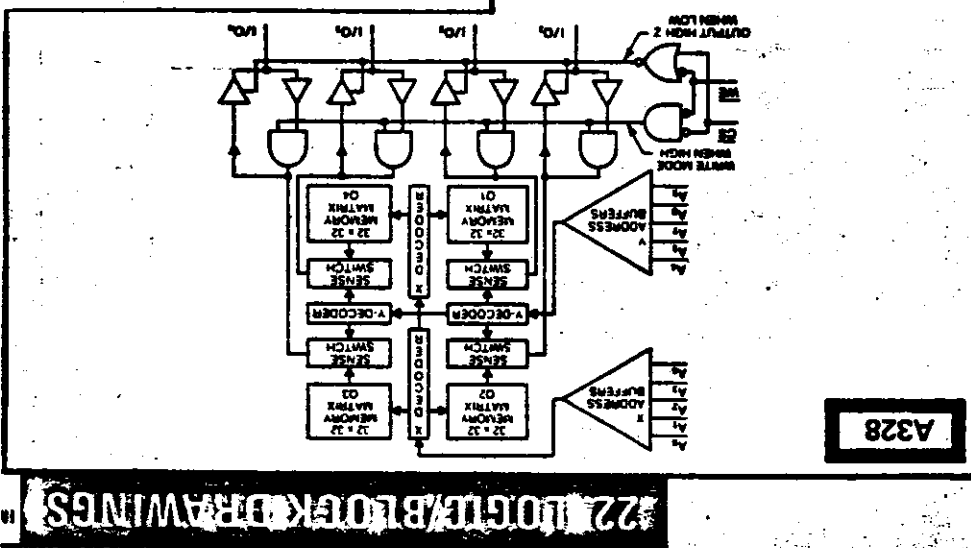
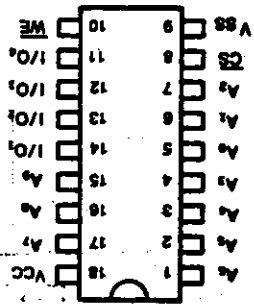
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TMS 4045
Sum as 2114



2114
1024 X 4 Static Ram
450 NS ACCESS
300 NS MAX WRITE
1 W DIV.
2.1 ma max. output sink



OVERVIEW OF I/O CIRCUITS

ROCKWELL

6500

MOTOROLA

6800

INTEL

8080

• PARALLEL
• 6520 PERIPHERAL INTERFACE
ADAPTOR

• 6820 PERIPHERAL
INTERFACE
ADAPTER

• 8212 8 BIT INPUT OR
OUTPUT PORT

• 6522 VERSATILE
INTERFACE ADAPTOR PIA

(PIA)

• 8255 PROGRAMMABLE
PERIPHERAL
INTERFACE

• 6530 MEM/IO/TIME

• 6532 MEM/IO/TIME

• SERIAL

• 6850 ASYNCHRONOUS
COMMUNICATIONS
INTERFACE
ADAPTOR

• 8251 PROGRAMMABLE
COMMUNICATION
INTERFACE

• 6852 SYNCHRONOUS SERIAL
DATA ADAPTOR

• 6860 DIGITAL MODEM

• 6862 2400 BPS MODEM MODULATOR

• 6863 2400 BPS MODEM DEMODULATOR

OVERVIEW OF I/O CIRCUITS

ROCKWELL	MOTOROLA	INTEL
6500	6800	8080

• INTERRUPT

NOTE: 6828 PRIORITY INTERRUPT 8214 PRIORITY INTERRUPT
MOTOROLA I/O CONTROLLER INTERRUPT
CIRCUITS ARE CONTROL UNIT
COMPATIBLE WITH
86500 BUS 8259 PROGRAMMABLE INTERRUPT CONTROLLER

• DIRECT MEMORY ACCESS

DMA CONTROLLER 8257 PROGRAMMABLE DMA CONTROLLER

OVERVIEW OF SUPPORT CIRCUITS

ROCKWELL

6500

MOTOROLA

6800

INTEL

8080

• CLOCK

NOTE: MOTOROLA CLOCK
AND PROGRAMMABLE
INTERFACE CIRCUITS
ARE COMPATIBLE WITH
R6500 BUS

• 6942 CLOCK DRIVER

• 8824 CLOCK GENERATOR

• 6870 CLOCK GENERATOR (HYBRID)

• 6871 CLOCK GENERATOR (HYBRID)

• 6875 CLOCK GENERATOR (MONOLITHIC)

• MISCELLANEOUS

• 6841 PROGRAMMABLE
INTERVAL
TIMER

• 8228 SYSTEM CONTROLLER

TIMER

• 8253 PROGRAMMABLE INTERVAL
TIMER

• 6881 TRIPLE BUS SWITCH

• 6848 8 X 8 MULTIPLEXER

8080B BENCHMARK COMPARISON TO INTEL 8085

APPLICATION	8085 (3 MHz)		6502A (2 MHz)		COMMENTS	
	PROGRAM BYTES	EXECUTION TIME	PROGRAM BYTES	EXECUTION TIME	8085	6502A
INCR/COMPARE 4-DIGIT COUNTER	26	34 μ SEC	23	18 μ SEC	DATA USUALLY IN MEMORY, OPERATIONS DONE IN REGISTERS	DATA IN ZERO PAGE
PROCESS I/O DATA	21	21 μ SEC	21	12 μ SEC	I/O ADDRESSING OPERATIONS DONE IN REGISTERS	ABSOLUTE ADDRESSED I/O MAY READ & PORT THICE TO GET SAME DATA
16-DIGIT BCD ADD	32	261 μ SEC	15	74 μ SEC	OPERATIONS DONE ON MEMORY DATA	OPERATIONS DONE ON ZERO PAGE DATA
0-BIT BINARY MULTIPLY	22	135 μ SEC	19	75 μ SEC	OPERATIONS DONE IN REGISTERS	REQUIRES ALL INTERNAL REGISTERS AND 1 ZERO PAGE LOCATION
INTERUPT SAVE/RESTORE	5	24 μ SEC	11	21 μ SEC	SAVES PC, ACC, PSW, HL PAIR	SAVES ALL CPU REGISTERS EXCEPT SP
STRING SEARCH	32	66 μ SEC	31	41 μ SEC	REFERENCE IS IN B,C,D; DATA IN MEMORY	DATA IS IN A FIXED MEMORY PAGE REF IS IN ZERO PAGE
BYTE SEARCH	16	926 μ SEC	12	412 μ SEC	DATA IN MEMORY	DATA IS IN A FIXED MEMORY PAGE REF IS IN ZERO PAGE
32 BIT BINARY MULTIPLY	30	547 μ SEC	33	274 μ SEC	DATA IN REGISTERS LOOP COUNTER IN MEMORY	DATA IS IN ZERO PAGE
10-BIT A/D CONVERSION	130	177 μ SEC	133	80 μ SEC	STRAIGHT-LINE PROGRAM HL ADDRESSED I/O	STRAIGHT-LINE PROGRAM ABSOLUTE ADDRESSED I/O

